9. (Amended) An integrated circuit structure comprising:

a semiconductor layer having a major surface formed along a plane;

first and second spaced-apart doped regions formed in the surface;

a third doped region over the first region of different conductivity type than the first region; and

a conductive layer formed between the first and second regions and above the plane, providing electrical connection between the doped regions, wherein the conductive layer comprises one or more materials taken from the group comprising tungsten silicide, tungsten nitride, titanium silicide, titanium nitride and cobalt silicide.

15. (Amended) A semiconductor device comprising:

a first layer of semiconductor material;

a first field effect transistor having a first source/drain region formed in the first layer, a channel region formed over the first layer and a second source/drain region formed over the channel region;

a second field effect transistor having a first source/drain region formed in the first layer, a channel region formed over the first layer and a second source/drain region formed over the channel region; and

a conductive layer in a plane extending between the first layer and the first field effect transistor channel region, said conductive layer comprising a metal positioned between the first source/drain region of each transistor to conduct current from one first source/drain region to the other first source/drain region.

19. (Amended) A semiconductor device comprising:

a first layer of semiconductor material;

a first field effect transistor having a first source/drain region formed in the first layer, a channel region formed over the first layer and a second source/drain region formed over the channel region;

a second field effect transistor having a first source/drain region formed in the first layer, a channel region formed over the first layer and a second source/drain region formed over the channel region; and